MEMORIES FOR ELECTRONIC SYSTEMS

ABSTRACT:

[0061] A switch 100 includes a plurality of ports 101 for exchanging data. A shared memory 102 enables the exchange of data between first and second ones of the ports 101 and includes an array 202 of memory cells arranged as a plurality of rows and a single column having width equal to a predetermined word-width and circuitry 202, 204, 206, 208 for writing selected data presented at the first one of the ports 101 to a selected row in the array as a word of the predetermined word-width during a first time period and for reading the selected data from the selected row as a word of the predetermined wordwidth during a second time period for output at a second one of the ports 101.